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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,340	03/24/2005	Armin Fischer	10808/229	8906

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EXAMINER	
HOLLINGTON, JERMELE M	

ART UNIT	PAPER NUMBER
2829	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,340	FISCHER ET AL.	
	Examiner	Art Unit	
	Jermele M. Hollington	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9,11-14 and 17-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *26* is/are allowed.

6)☒ Claim(s) *1,3-7,9,11-14 and 17-25* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The following guidelines illustrate the layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

1. The disclosure is objected to because of the following informalities: there are no section heading in the disclosure such as TITLE OF THE INVENTION, BACKGROUND OF THE INVENTION, BRIEF SUMMARY OF THE INVENTION, BRIEF DESCRIPTION OF THE

SEVERAL VIEWS OF THE DRAWING(S), DETAILED DESCRIPTION OF THE INVENTION, and CLAIM OR CLAIMS.

Appropriate correction is required.

Claim Objections

2. Claim 1 is objected to because of the following informalities: in line 2 of the amending claim 1, the limitation "a integrated circuit" should be change to --an integrated circuit--. Furthermore, the disclosure does not show an integrated circuit substrate. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-7, 9, 11-14, 17-18 and 20-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Snyder et al (5625288).

Regarding claims 1 and 13, Snyder et al disclose [see Fig. 19] an integrated test circuit arrangement having integrated test structures (DUT 26) [see col. 3, lines 48-53] located on an integrated circuit substrate, at least one integrated heating element (heating element 28) located on the integrated circuit, an integrated detection unit (buffer 24) which detects at least one physical property for each of the test structures (26), an integrated supply unit (oscillator 22), located on the integrated circuit substrate, which supplies each of the test structure (26) with a

current or a voltage in switchable fashion independently of one another [see col. 3, lines 9-13 and 46-48], and a control unit (external DC control means 35) which is connected to outputs of the detection unit (22) on an input side and which controls the supply unit (22) dependent on the detection results.

Regarding claims 3 and 18, Snyder et al disclose wherein the test structures (26) of a first group have the same construction among one another.

Regarding claim 4, Snyder et al disclose wherein at least one of: the supply unit (22) contains at least one of: a multiplicity of integrated current sources and a multiplicity of integrated voltage sources, and the current sources contain a plurality of current mirrors which generate a multiple or a fraction of a reference current or a current having the magnitude of the reference current [see col. 3, line 56- col. 4, line 18].

Regarding claim 5, Snyder et al disclose the heating element (28) at least one of: contains a resistance heating element which comprises monocrystalline silicon or polycrystalline silicon or which comprises a metal [see col. 5, lines 21-44], and has a straight profile, a meandering profile, a triangular function profile or a rectangular function profile.

Regarding claim 6, Snyder et al disclose at least one reference structure (current controlled oscillator ICO), at least one of the construction and the dimensions of which differ from the construction and the dimensions of the test structures (26).

Regarding claim 7, Snyder et al disclose wherein the detection unit (24) at least one of: is connected or can be connected to the test structures (26), and contains at least one counter, which is clocked in accordance with a predetermined clock.

Regarding claim 9, Snyder et al disclose the control unit (35) outputs at least one of: detection results, a datum for ascertaining the detection instant and which, datum for identifying the test structures (26).

Regarding claim 11, Snyder et al disclose electronic components (30) associated with a user circuit (35).

Regarding claim 12, Snyder et al disclose wherein the circuit arrangement (102) is encapsulated in a plastic housing or in a ceramic housing (not numbered but shown).

Regarding claim 14, Snyder et al disclose comprising at least one of the following steps: integrating at least one heating element (28) into the integrated circuit arrangement, warming or heating the test structures (26) with the aid of the heating element (28), and connecting the supply unit (35) to the test structure (28) during warming or during heating.

Regarding claim 17, Snyder et al disclose further comprising the following steps: integrating at least one reference structure (current controlled oscillator ICO), at least one of the construction and the dimensions of which differ from the construction and the dimensions of the test structures (26), detecting one of the physical reference properties at the reference structure (ICO), comparing (via 302) the one of the physical properties with the reference property or comparing (via 302) a quantity generated from the one of the physical properties and a quantity generated from the reference property.

Regarding claim 20, Snyder et al disclose an output circuit (output) is integrated into the integrated circuit arrangement, the output circuit (output) outputs at least one set of detection data for the test structures (26).

Regarding claim 21, Snyder et al disclose at least one of: an integrated circuit arrangement that is still arranged on a semiconductor wafer (not numbered), the semiconductor wafer (not numbered) carrying a multiplicity of other integrated circuit arrangements (26), and in that the method for the purpose of monitoring ongoing production.

Regarding claim 22, Snyder et al disclose integrating at least a part of the supply unit (35) into the integrated circuit arrangement (26), said part containing at least one active component.

Regarding claim 23, Snyder et al disclose the test structures (26) of a second group contain interconnects which at least one of: comprise a metal or are led into another metallization layer by means of a via, the test structures (26) of a third group contain dielectrics, or the test structures (26) of a fourth group contain active or passive electronic components.

Regarding claim 24, Snyder et al disclose the electronic components comprise at least one of a memory unit and a processor (shown not numbered).

Regarding claim 25, Snyder et al disclose registering an instant at which the comparison result changes.

Conclusion

Response to Arguments

5. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

6. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claim 26 is allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 8 and 26, the primary reason for the allowance of the claim is due the detection unit contains at least one multiplexer unit, the inputs of which are electrically connected to a respective test structure, and in that the an output of the multiplexer unit is connected to the first input of a comparison unit, the second input of which is electrically connected to a reference structure, the reference structure having at least one of a different construction and different dimensions than a-the test structures.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jermele M. Hollington whose telephone number is (571) 272-1960. The examiner can normally be reached on M-F (9:00-4:00 EST) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on (571) 272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jermele M. Hollington
Primary Examiner
Art Unit 2829

JMH
May 31, 2007